AAT1149

SwitchReg™

3MHz Fast Transient 400mA Step-Down Converter

General Description

The AAT1149 SwitchReg is a 3.0MHz step-down converter with an input voltage range of 2.7V to 5.5V and output voltage as low as 1.0V. It is optimized to react quickly to load variations and operate with a tiny 0603 inductor that is only 1mm tall.

The AAT1149 output voltage is programmable via external feedback resistors. It can deliver 400mA of load current while maintaining a low 45µA no load quiescent current. The 3.0MHz switching frequency minimizes the size of external components while keeping switching losses low.

The AAT1149 maintains high efficiency throughout the operating range, which is critical for portable applications.

The AAT1149 is available in a Pb-free, space-saving 2.0x2.1mm SC70JW-8 package or a 5-pin wafer-level chip scale (WLCSP) package and is rated over the -40°C to +85°C temperature range.

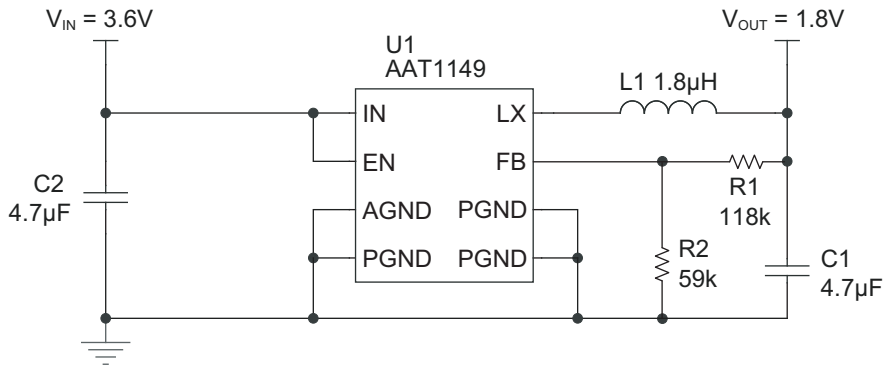
Features

- Ultra-Small 0603 Inductor (Height = 1mm)
- V_{IN} Range: 2.7V to 5.5V
- V_{OUT} Adjustable from 1.0V to V_{IN}
- 400mA Max Output Current
- Up to 98% Efficiency
- 45µA No Load Quiescent Current
- 3.0MHz Switching Frequency
- 70µs Soft Start
- Fast Load Transient
- Over-Temperature Protection
- Current Limit Protection
- 100% Duty Cycle Low-Dropout Operation
- <1µA Shutdown Current
- SC70JW-8 or 0.9x1.2mm WLCSP Package
- Temperature Range: -40°C to +85°C

Applications

- Cellular Phones
- Digital Cameras
- Handheld Instruments
- Microprocessor / DSP Core / IO Power
- PDAs and Handheld Computers
- USB Devices

Typical Application

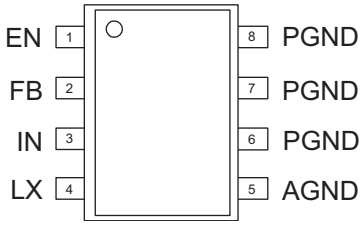


Pin Descriptions

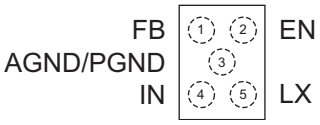
Pin # SC70JW-8	Pin # WLCSP	Symbol	Function
1	2	EN	Enable pin.
2	1	FB	Feedback input pin. This pin is connected to an external resistive divider for an adjustable output.
3	4	IN	Input supply voltage for the converter.
4	5	LX	Switching node. Connect the inductor to this pin. It is internally connected to the drain of both high- and low-side MOSFETs.
5	3	AGND	Non-power signal ground pin.
6, 7, 8		PGND	Main power ground return pins. Connect to the output and input capacitor return.

Pin Configuration

SC70JW-8
(Top View)



WLCSP-5
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{IN}	Input Voltage to GND	6.0	V
V_{LX}	LX to GND	-0.3 to V_{IN} + 0.3	V
V_{FB}	FB to GND	-0.3 to V_{IN} + 0.3	V
V_{EN}	EN to GND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information

Symbol	Description		Value	Units
P_D	Maximum Power Dissipation	SC70JW-8[2, 3]	625	mW
		WLCSP-5[2, 4]	352	
θ_{JA}	Thermal Resistance[2]	SC70JW-8	160	°C/W
		WLCSP-5	284	

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board; for the WLCSP package, use the NSMD (none-solder mask defined) pad style for tighter control on the copper etch process.
3. Derate 6.25mW/°C above 25°C.
4. Derate 3.52 mW/°C above 25°C.

Electrical Characteristics[1]

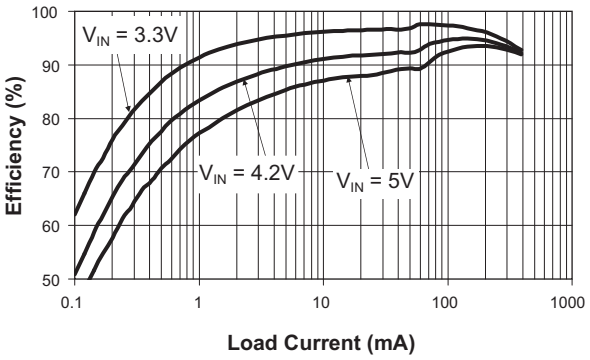
V_{IN} = 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
Step-Down Converter						
V_{IN}	Input Voltage		2.7		5.5	V
		V_{IN} Rising			2.7	V
V_{UVLO}	UVLO Threshold	Hysteresis		100		mV
		V_{IN} Falling	1.8			V
V_{OUT}	Output Voltage Tolerance	I_{OUT} = 0 to 400mA, V_{IN} = 2.7V to 5.5V	-3.0		3.0	%
V_{OUT}	Adjustable Output Voltage Range		1.0		V_{IN}	V
I_Q	Quiescent Current	No Load		45	70	µA
I_{SHDN}	Shutdown Current	V_{EN} = GND			1.0	µA
I_{LIM}	P-Channel Current Limit		600			mA
$R_{DS(ON)H}$	High Side Switch On Resistance	SC70JW-8		0.45		Ω
		WLCSP-5		0.40		
$R_{DS(ON)L}$	Low Side Switch On Resistance	SC70JW-8		0.40		Ω
		WLCSP-5		0.35		
I_{LXLEAK}	LX Leakage Current	V_{IN} = 5.5V, V_{LX} = 0 to V_{IN}, V_{EN} = GND			1	µA
$\Delta V_{Linereg}$	Line Regulation	V_{IN} = 2.7V to 5.5V		0.1		%/V
V_{OUT}	Out Threshold Voltage Accuracy	0.6V Output, No Load, T_A = 25°C	591	600	609	mV
I_{OUT}	Out Leakage Current	0.6V Output			0.2	µA
T_S	Start-Up Time	From Enable to Output Regulation		70		µs
F_{OSC}	Oscillator Frequency	T_A = 25°C		3.0		MHz
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
EN						
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.4			V
I_{EN}	Input Low Current	V_{IN} = V_{OUT} = 5.5V	-1.0		1.0	µA

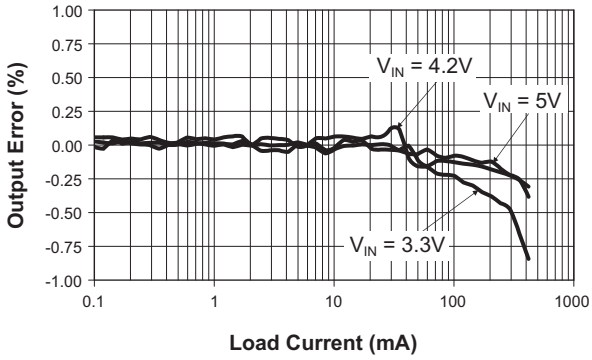
1. The AAT1149 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Typical Characteristics

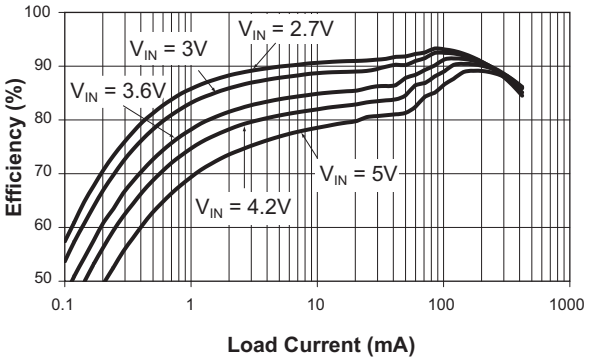
Efficiency vs. Load Current
(V_{OUT} = 3V; L = 3µH)



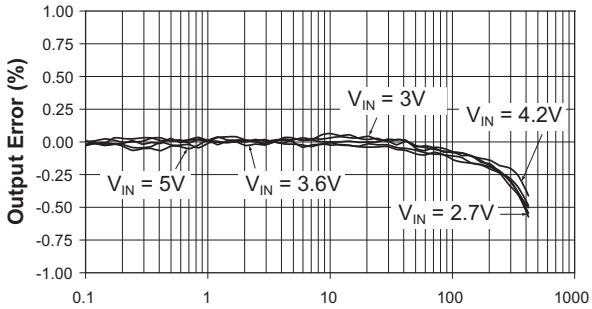
Load Regulation
(V_{OUT} = 3V; L = 3µH)



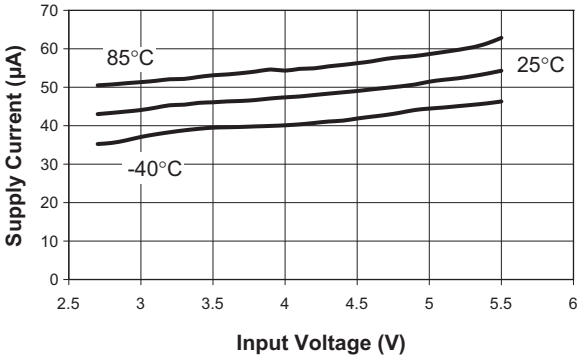
Efficiency vs. Load Current
(V_{OUT} = 1.8V; L = 2.2µH)



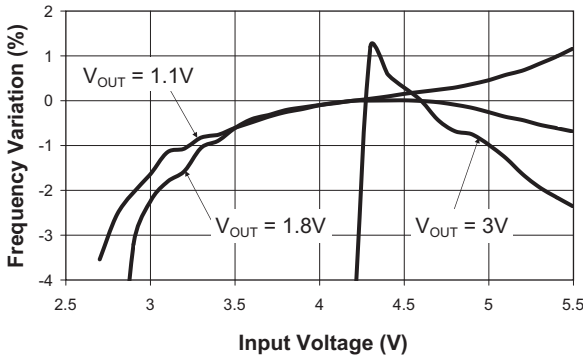
Load Regulation
(V_{OUT} = 1.8V; L = 2.2µH)



No Load Quiescent Current vs. Input Voltage

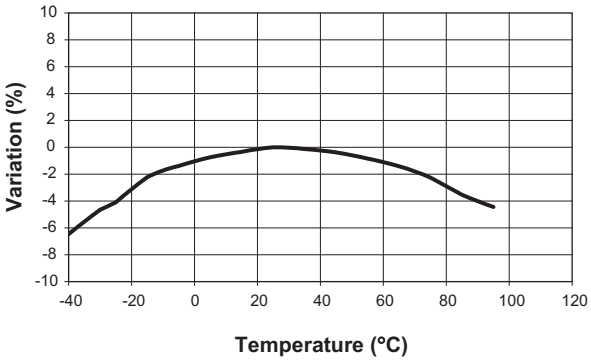


Switching Frequency vs. Input Voltage



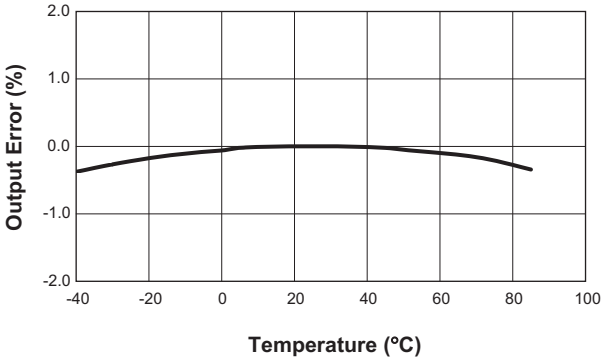
Typical Characteristics

Switching Frequency Variation vs. Temperature



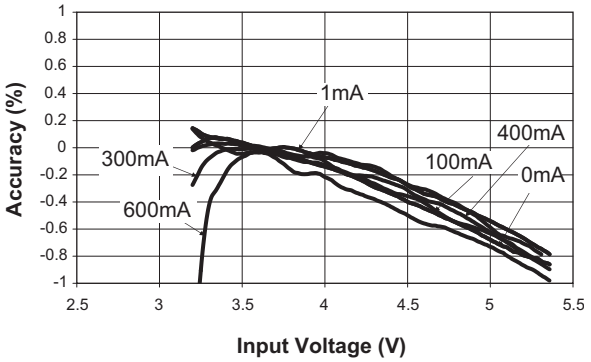
Output Voltage Error vs. Temperature

(V_{IN} = 3.6V; V_O = 1.8V; I_{OUT} = 400mA)



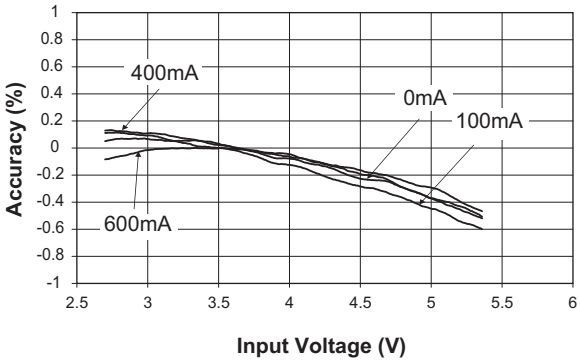
Line Regulation

(V_{OUT} = 3V)



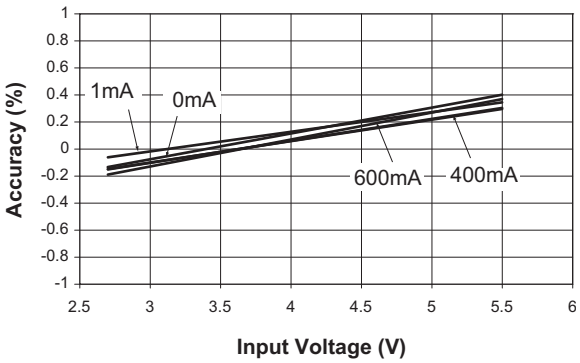
Line Regulation

(V_{OUT} = 1.8V)



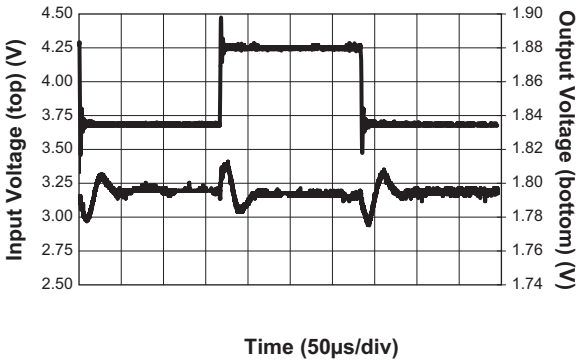
Line Regulation

(V_{OUT} = 1.1V)



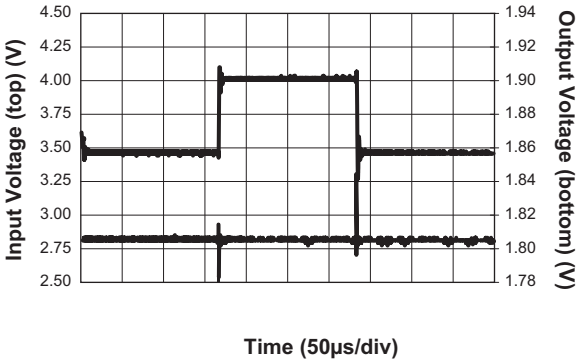
Line Transient

(V_{OUT} = 1.8; 400mA Load; No Feedforward Capacitor)

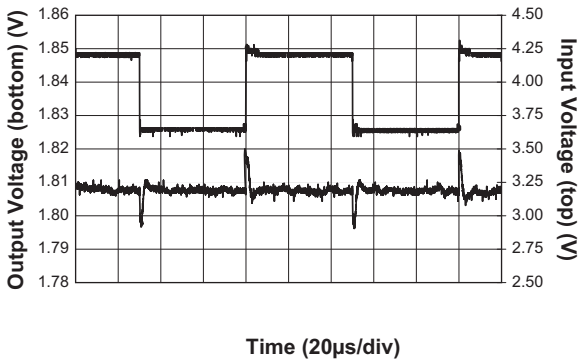


Typical Characteristics

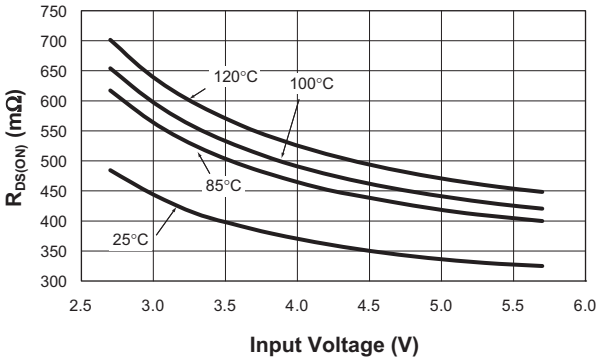
Line Transient
(V_{OUT} = 1.8; No Load; No Feedforward Capacitor)



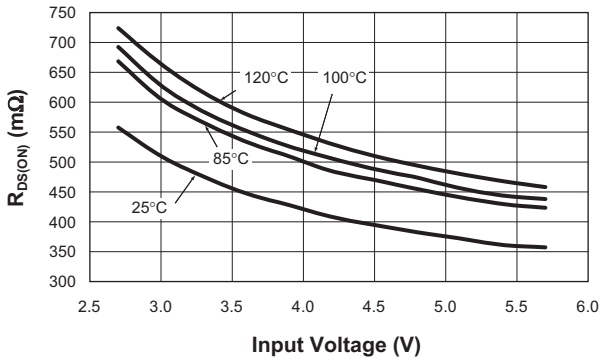
Line Transient
(V_{OUT} = 1.8; C_{FF} = 100pF)



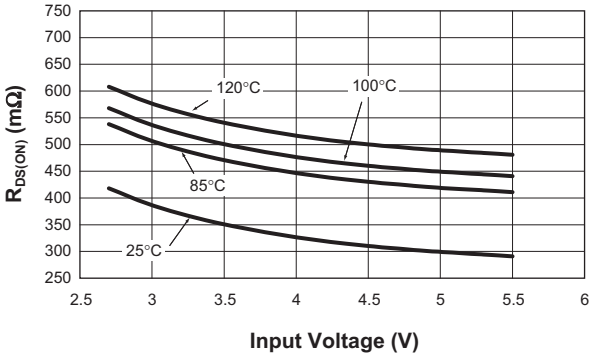
N-Channel $R_{DS(ON)}$ vs. Input Voltage
(SC70JW-8)



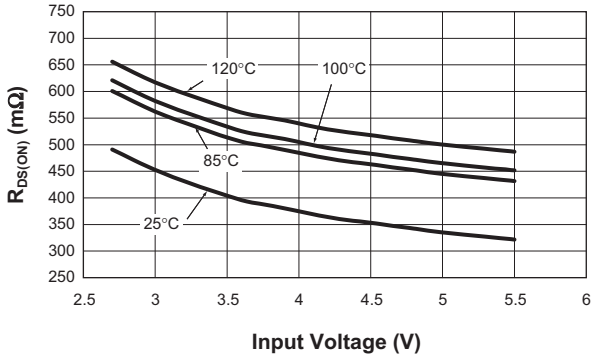
P-Channel $R_{DS(ON)}$ vs. Input Voltage
(SC70JW-8)



N-Channel $R_{DS(ON)}$ vs. Input Voltage
(WLCSP-5)

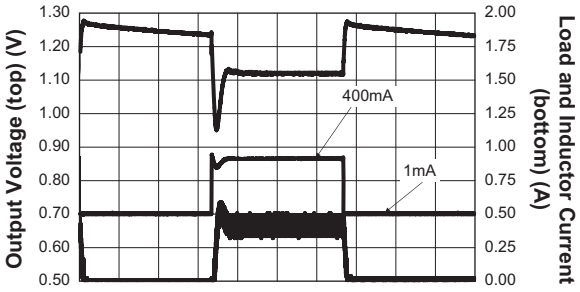


P-Channel $R_{DS(ON)}$ vs. Input Voltage
(WLCSP-5)



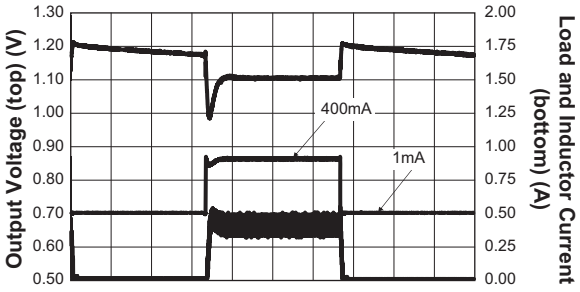
Typical Characteristics

Load Transient
(V_{OUT} = 1.1V; No Feedforward Capacitor)



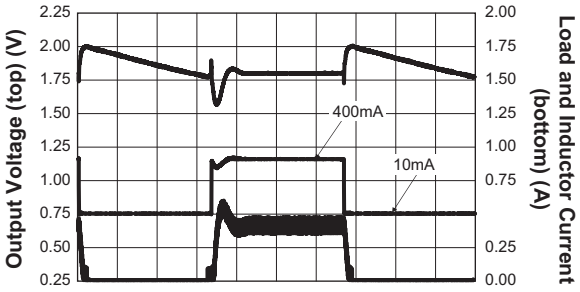
Time (50µs/div)

Load Transient
(V_{OUT} = 1.1V; C_{FF} = 100pF)



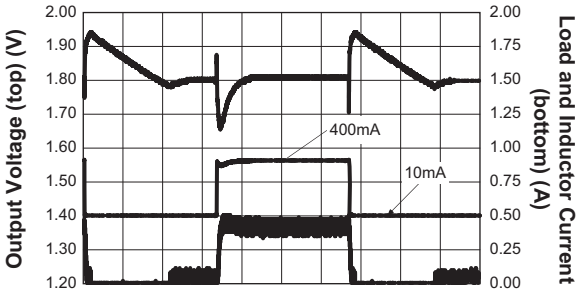
Time (50µs/div)

Load Transient
(V_{OUT} = 1.8V; No Feedforward Capacitor)



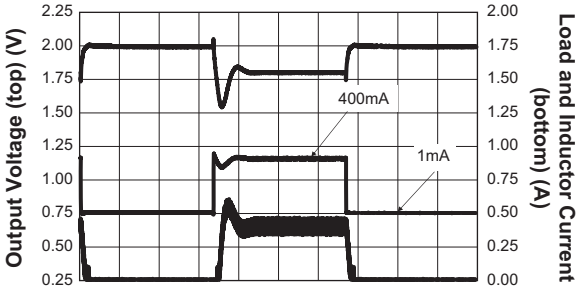
Time (50µs/div)

Load Transient
(V_{OUT} = 1.8V; C_{FF} = 100pF)



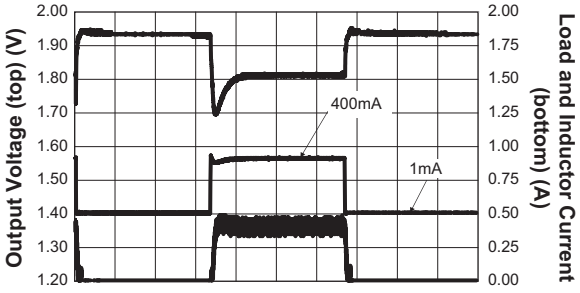
Time (50µs/div)

Load Transient
(V_{OUT} = 1.8V; No Feedforward Capacitor)



Time (50µs/div)

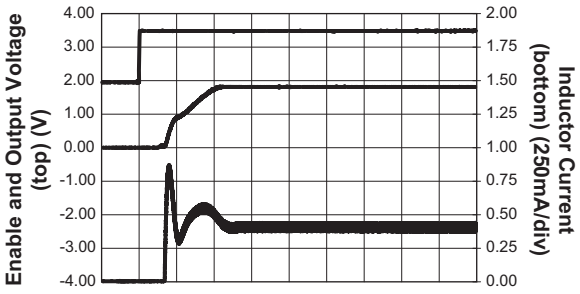
Load Transient
(V_{OUT} = 1.8V; C_{FF} = 100pF)



Time (50µs/div)

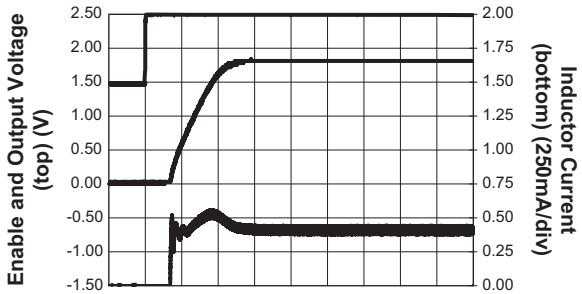
Typical Characteristics

Soft Start
(V_{OUT} = 1.8V; No Feedforward Capacitor)



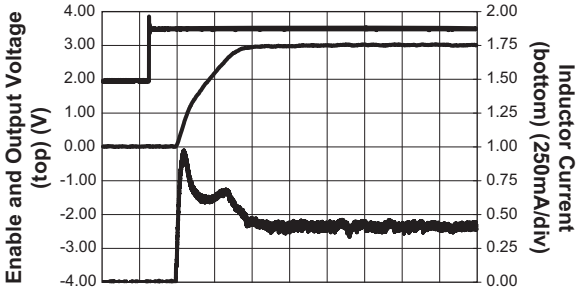
Time (50µs/div)

Soft Start
(V_{OUT} = 1.8V; C_{FF} = 100pF)



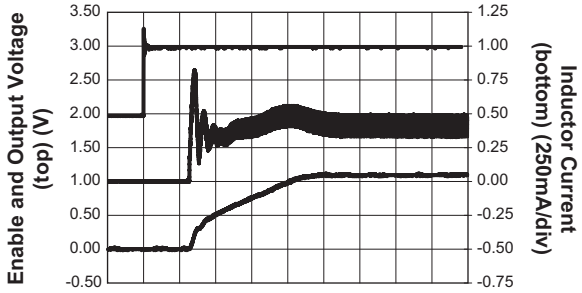
Time (50µs/div)

Soft Start
(V_{OUT} = 3V; No Feedforward Capacitor)



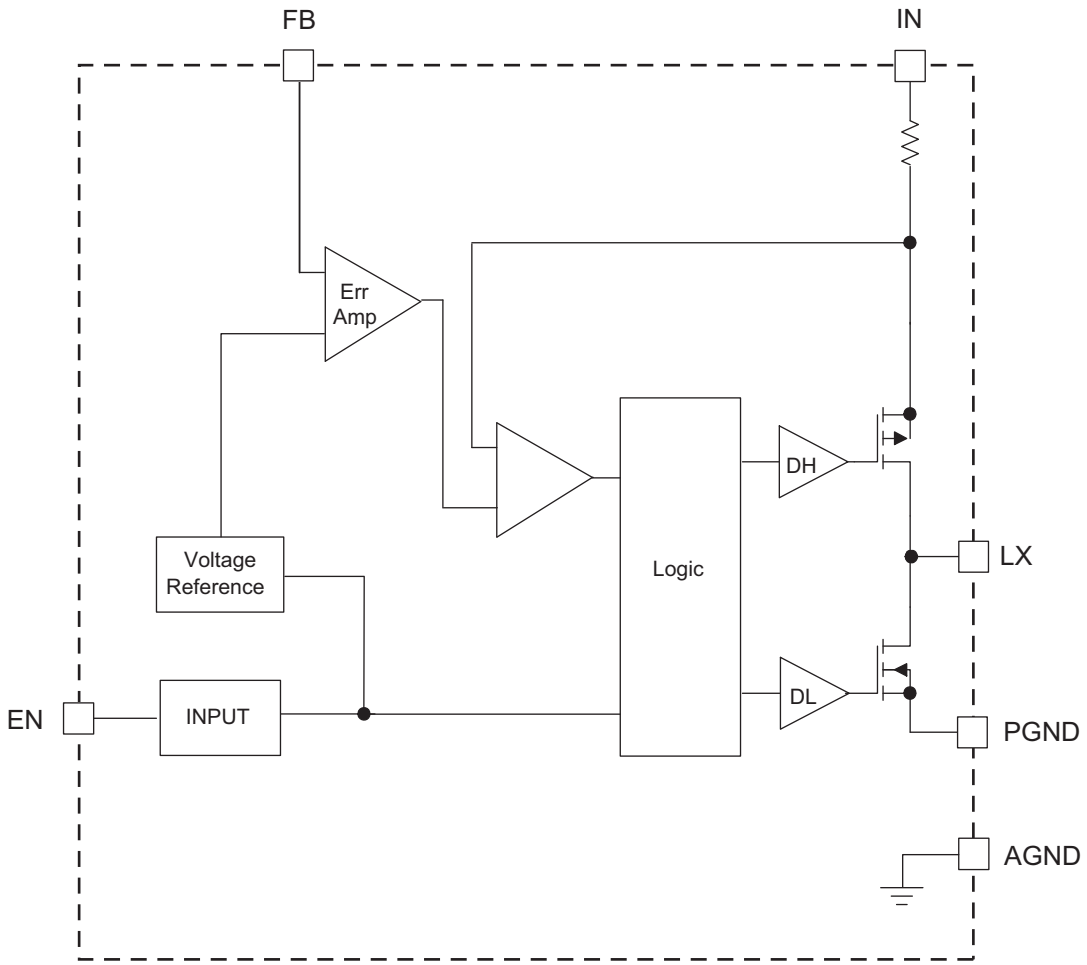
Time (50µs/div)

Soft Start
(V_{OUT} = 1.1V; No Feedforward Capacitor)



Time (20µs/div)

Functional Block Diagram



Functional Description

The AAT1149 is a high performance 400mA 3.0MHz monolithic step-down converter. It minimizes external component size, enabling the use of a tiny 0603 inductor that is only 1mm tall, and optimizes efficiency over the complete load range. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. Typically, a 1.8µH inductor and a 4.7µF ceramic capacitor are recommended (see table of values).

Only three external power components (C_{IN}, C_{OUT}, and L) are required. Output voltage is programmed with external feedback resistors, ranging from 1.0V to the input voltage. An additional feed-forward capacitor can also be added to the external feedback to provide improved transient response (see Figure 4).

At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the $R_{DS(ON)}$ drop of the P-channel high-side MOSFET.

The input voltage range is 2.7V to 5.5V. The converter efficiency has been optimized for all load conditions, ranging from no load to 400mA.

The internal error amplifier and compensation provides excellent transient response, load, and line regulation. Soft start eliminates any output voltage overshoot when the enable or the input voltage is applied.

Control Loop

The AAT1149 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. For the adjustable output, the error amplifier reference is fixed at 0.6V.

Soft Start / Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When pulled low, the enable input forces the AAT1149 into a low-power, non-switching state. The total input current during shutdown is less than 1µA.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles.

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled via the IN input. Under-voltage lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry prior to activation.

Applications Information

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. Table 1 displays suggested inductor values for various output voltages.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 1.8µH CDRH2D09 series inductor selected from Sumida has a 131mW DCR and a 400mA saturation current rating. At full load, the inductor DC loss is 21mW which gives a 2.8% loss in efficiency for a 400mA, 1.8V output.

Input Capacitor

Select a 4.7µF to 10µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

Configuration	Output Voltage	Typical Inductor Value
0.6V Adjustable With External Feedback	1V, 1.2V	1.0µH to 1.2µH
	1.5V, 1.8V	1.5µH to 1.8µH
	2.5V	2.2µH to 2.7µH
	3.3V	3.3µH

Table 1: Inductor Values.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT1149. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C2) can be seen in the evaluation board layout in Figure 1.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7µF to 10µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

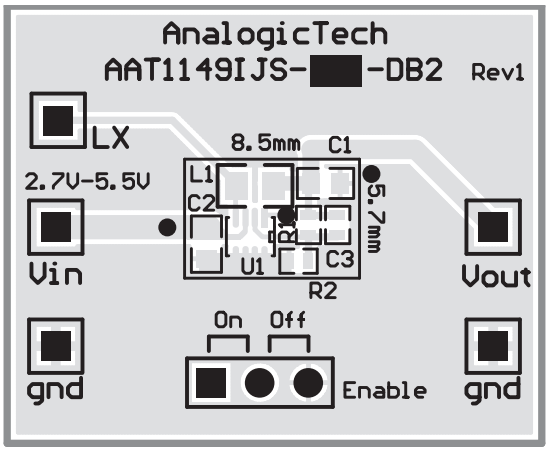


Figure 1: AAT1149IJS Evaluation Board Top Side.

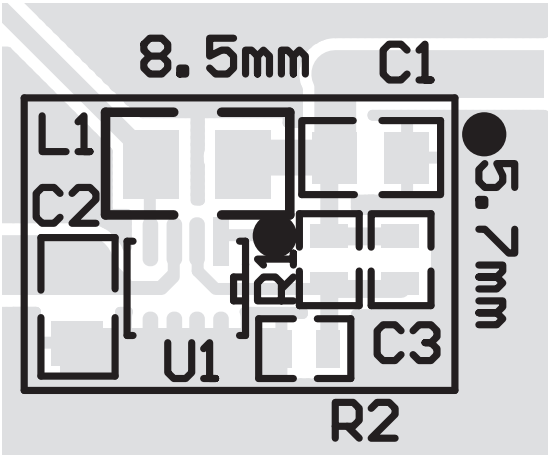


Figure 2: Exploded View of Evaluation Board Top Side.

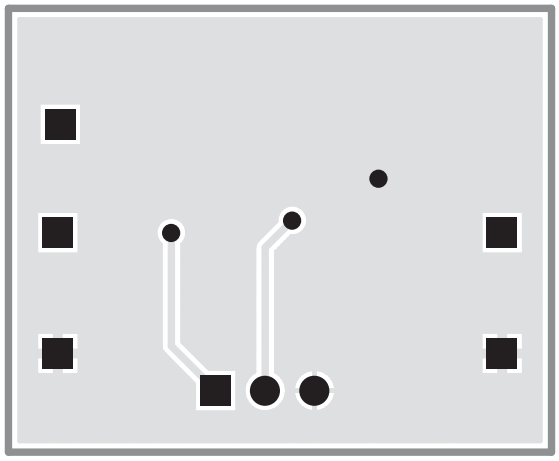


Figure 3: AAT1149IJS Evaluation Board Bottom Side.

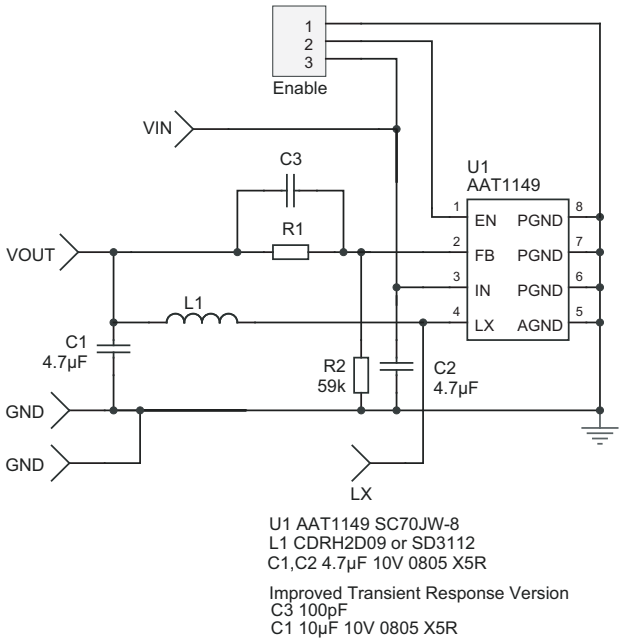


Figure 4: AAT1149IJS Evaluation Board Schematic.

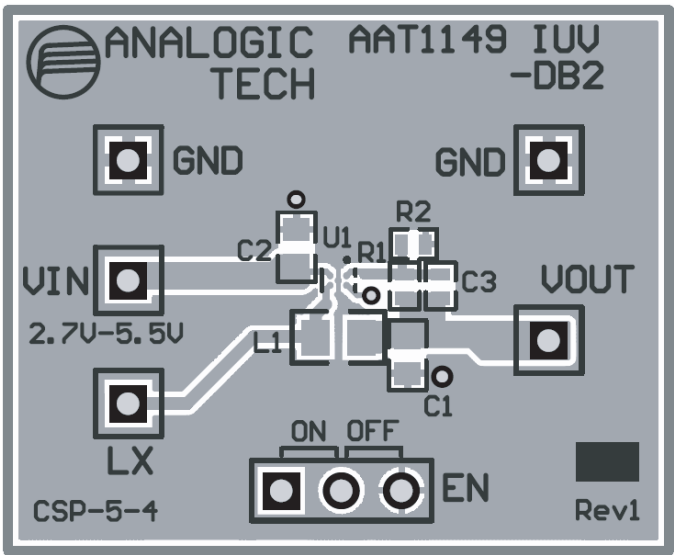


Figure 5: AAT1149IUV Evaluation Board Top Side.

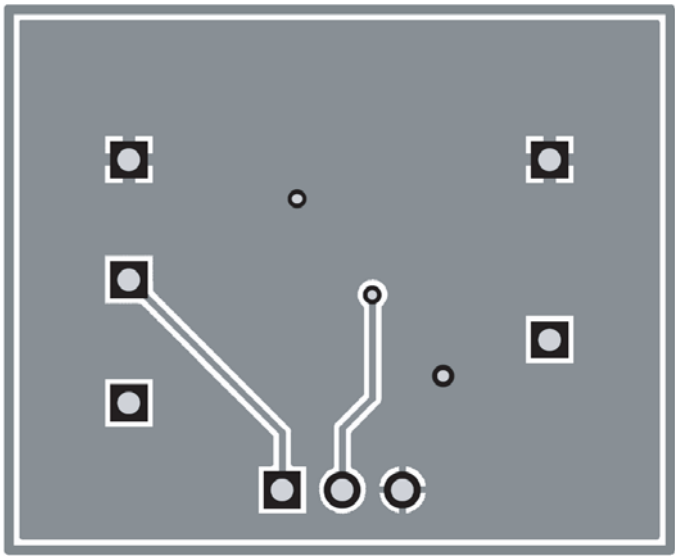


Figure 6: AAT1149IUV Evaluation Board Bottom Side.

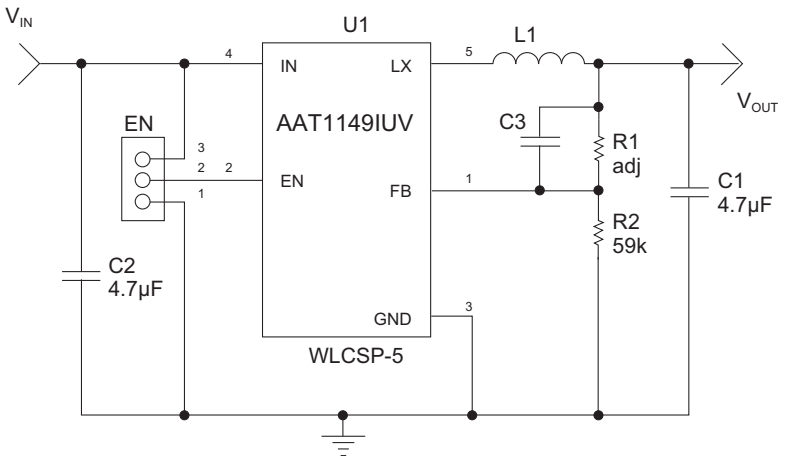


Figure 7: AAT1149IUV Evaluation Board Schematic.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

Feedback Resistor Selection

Resistors R1 and R2 of Figure 4 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 2 summarizes the resistor values for various output voltages with R2 set to either 59kΩ for good noise immunity or 221kΩ for reduced no load input current.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \cdot R2 = \left(\frac{1.5V}{0.6V} - 1\right) \cdot 59k\Omega = 88.5k\Omega$$

The AAT1149, combined with an external feedforward capacitor (C3 in Figure 4), delivers enhanced transient response for extreme pulsed load applications. The addition of the feedforward capacitor typically requires a larger output capacitor C1 for stability.

V_{OUT} (V)	R2 = 59kΩ R1 (kΩ)	R2 = 221kW R1 (kΩ)
0.9	29.4	113K
1.0	39.2	150K
1.1	49.9	187K
1.2	59.0	221K
1.3	68.1	261K
1.4	78.7	301K
1.5	88.7	332K
1.8	118	442K
1.85	124	464K
2.0	137	523K
2.5	187	715K
3.3	267	1.00M

Table 2: Feedback Resistor Values.

Thermal Calculations

There are three types of losses associated with the AAT1149 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_O + R_{DS(ON)L} \cdot [V_{IN} - V_O])}{V_{IN}}$$

$$+ (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)H} + I_Q \cdot V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the SC70JW-8 package which is 160°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

WLCSP Package Light Sensitivity

The electrical performance of the WLCSP package can be adversely affected by exposing the device to certain light sources such as direct sunlight or a halogen lamp whose wavelengths are red and infra-reds. However, fluorescent lighting has very little effect on the electrical performance of the WLCSP package.

Layout

The suggested PCB layout for the AAT1149 is shown in Figures 1, 2, and 3. The following guidelines should be used to help ensure a proper layout.

1. The input capacitor (C2) should connect as closely as possible to IN (Pin 3) and PGND (Pins 6-8).
2. C1 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible.
3. The feedback trace or FB pin (Pin 2) should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin (Pin 2) to minimize the length of the high impedance feedback trace.
4. The resistance of the trace from the load return to the PGND (Pins 6-8) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. The pad on the PCB for the WLCSP-5 package should use NSMD (non-solder mask defined) configuration due to its tighter control on the copper etch process. A pad thickness of less than 1oz is recommended to achieve higher stand-off. A high density, small footprint layout can be achieved using an inexpensive, miniature, non-shielded, high DCR inductor, as shown in Figure 8.

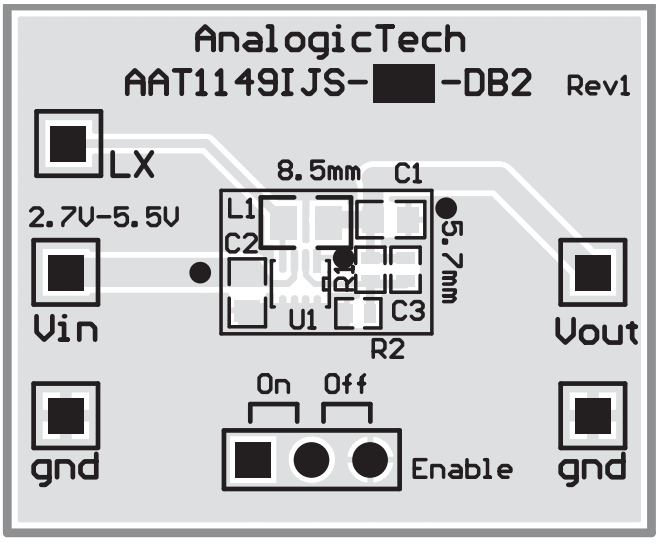


Figure 8: Minimum Footprint Evaluation Board Using 2.0x1.25x1.0mm Inductor.

Step-Down Converter Design Example

Specifications

V_O = 1.8V @ 400mA (adjustable using 0.6V version), Pulsed Load DI_{LOAD} = 300mA

V_{IN} = 2.7V to 4.2V (3.6V nominal)

F_S = 3.0MHz

T_{AMB}=85°C

1.8V Output Inductor

$$L1 = 1\frac{\mu s}{A} \cdot V_O = 1\frac{\mu s}{A} \cdot 1.8V = 1.8\mu H$$ (use 2.2µH; see Table 1)

For Taiyo Yuden inductor CBC2518T2R2M, 2.2µH, DCR = 130mΩ.

$$\Delta I_{L1} = \frac{V_O}{L1 \cdot F_S} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1.8V}{2.2\mu H \cdot 3.0MHz} \cdot \left(1 - \frac{1.8V}{4.2V}\right) = 156mA$$

$$I_{PKL1} = I_O + \frac{\Delta I_{L1}}{2} = 0.4A + 0.078A = 0.478A$$

$$P_{L1} = I_O^2 \cdot DCR = 0.4A^2 \cdot 130m\Omega = 21mW$$

1.8V Output Capacitor

V_{DROOP} = 0.1V

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.3A}{0.1V \cdot 3.0MHz} = 3.0\mu F; \text{ use } 4.7\mu F$$

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_O) \cdot (V_{IN(MAX)} - V_O)}{L1 \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.8V \cdot (4.2V - 1.8V)}{2.2\mu H \cdot 3.0MHz \cdot 4.2V} = 45mArms$$

$$P_{esr} = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (45mA)^2 = 10\mu W$$

Input Capacitor

Input Ripple V_{PP} = 25mV

$$C_{IN} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{25mV}{0.4A} - 5m\Omega\right) \cdot 4 \cdot 3.0MHz} = 1.45\mu F; \text{ use } 2.2\mu F$$

$$I_{RMS} = \frac{I_O}{2} = 0.2Arms$$

$$P = esr \cdot I_{RMS}^2 = 5m\Omega \cdot (0.2A)^2 = 0.2mW$$

AAT1149 Losses (SC70JW-8 Package)

$$P_{TOTAL} = \frac{I_O^2 \cdot (R_{DS(ON)H} \cdot V_O + R_{DS(ON)L} \cdot [V_{IN} - V_O])}{V_{IN}} + (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

$$= \frac{0.4^2 \cdot (0.725\Omega \cdot 1.8V + 0.7\Omega \cdot [4.2V - 1.8V])}{4.2V} + (5ns \cdot 3MHz \cdot 0.4A + 70\mu A) \cdot 4.2V = 140mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 85°C + (160°C/W) \cdot 140mW = 107°C$$

Adjustable Version (0.6V device) V_{OUT} (V)	R2 = 59kΩ1 R1 (kΩ)	R2 = 221kΩ1 R1 (kΩ)	L1 (µH)
1.0	39.2	150	1.0
1.2	59.0	221	1.2
1.5	88.7	332	1.5
1.8	118	442	1.8
2.5	187	715	2.2
3.3	267	1000	3.3

Table 3: Evaluation Board Component Values.

Manufacturer	Part Number/Type	Inductance (µH)	Rated Current (mA)	DCR (Ω)	Size (mm) LxWxH
Taiyo Yuden	BRC1608	0.77	660	110	0603 (H_{MAX} = 1mm)
		1.0	520	180	
		1.5	410	300	
	BRL2012	1.5	600	200	0805 (H_{MAX} = 1mm)
		2.2	550	250	
		3.3	450	350	
	CBC2518 Wire Wound Chip	1.0	1000	80	2.5x1.8x1.8
		2.2	890	130	
Sumida	CDRH2D09 Shielded	1.2	590	97.5	3.2x3.2x1.0
		1.5	520	110	
		1.8	480	131	
		2.5	440	150	
		3.0	400	195	
Murata	LQH2MCN4R7M02 Unshielded	1.0	485	300	2.0x1.6x0.95
		1.5	445	400	
		2.2	425	480	
		3.3	375	600	
Coiltronics	SD3118 Shielded	0.68	980	31	3.15x3.15x1.2
		0.82	830	54	
		1.2	720	75	
		1.5	630	104	
		2.2	510	116	
		3.3	430	139	

Table 4: Typical Surface Mount Inductors.

Manufacturer	Part Number	Value	Voltage	Temp. Co.	Case
Murata	GRM219R61A475KE19	4.7µF	10V	X5R	0805
Murata	GRM21BR60J106KE19	10µF	6.3V	X5R	0805
Murata	GRM185R60J475M	4.7µF	6.3V	X58	0603

Table 5: Surface Mount Capacitors.

1. For reduced quiescent current, R2 = 221kΩ.

Ordering Information

Output Voltage[1]	Package	Marking[2]	Part Number (Tape and Reel)[3, 4]
0.6; Adj ≥ 1.0	SC70JW-8	RGXYY	**AAT1149IJS-0.6-T1**
0.6; Adj ≥ 1.0	WLCSP-5	RGYW[5]	**AAT1149IUV-0.6-T1**

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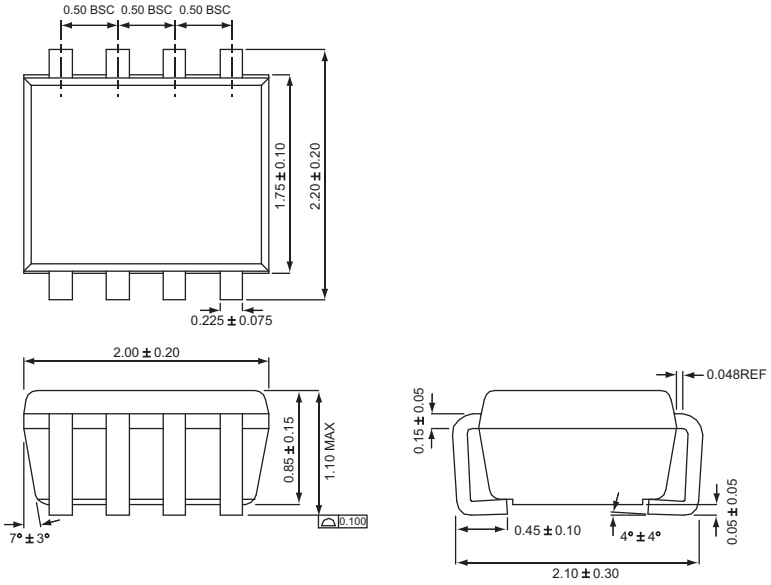
Package Information

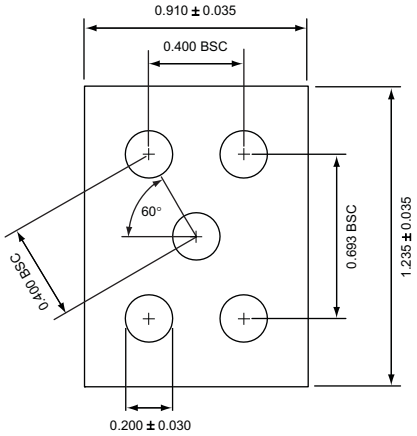
SC70JW-8



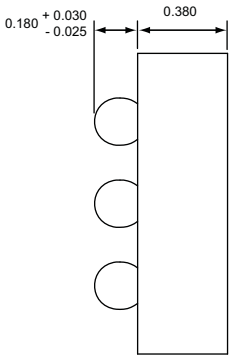
All dimensions in millimeters.

1. Contact Sales for other voltage options.
2. XYY = assembly and date code.
3. Sample stock is generally held on part numbers listed in **BOLD**.
4. Available exclusively outside of the United States and its territories.
5. YW = date code (year, week) for WLCSP-5 package.

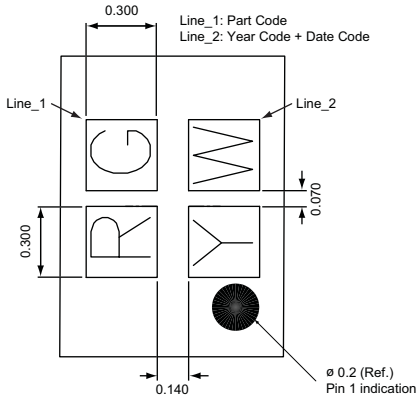
WLCSP-5



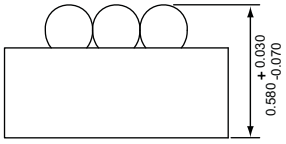
Bottom View



Side View



Top View



End View

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